$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m V_{gs}}{V_{in}} = \frac{g_m}{R_{in}\omega_0 C_t} \quad (6)$$

Where ω_0 is operation frequency. Thus, the power across the load can be written as

$$P_0 = \frac{V_{out}^2}{R_{load}} = \frac{\left[I_{out} \cdot (R_{load} \,//\, R_{out}) V_{gs}\right]^2}{R_{load}} = \frac{g_m}{R_{in}\omega_0 C_t} \quad (7)$$

The power gain is approximately presented as

$$G_c = \frac{P_o}{P_i} = \left[G_m \frac{R_{out}}{R_{load} + R_{out}}\right]^2 \cdot R_{load} \quad (8)$$

3.3 Folded-cascode Mixers

On the basis of formulas proposed by Friis [13], noise could be lower, and gain could be higher for increasing stages of series system. In the receiver system, the noise made by Mixer could be suppressed by high gain LNA. For analysing flicker noise inside Mixer, we divided Mixer to 3 components including RF input gain stage, LO switching stage and IF load. Poly-silicon resistors are used for IF load with less flicker noise. Gain stage input and flicker noise of RF input signal are frequency shifting in a switch stage. Based on the principle of Mixer, flicker noise will be transferred to LO frequency or to other band whose central frequency is odd. And it won't be shown on a baseband. Flicker noise of the whole system is caused by LO switching stage in Mixer [8-9]. The flicker noise current is expressed as

$$\overline{i_n^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \approx \frac{K}{f} \cdot \omega_T^2 \cdot A \cdot \Delta f \quad (9)$$

K is process parameter and *A (=W*L)* is Gate size. From Equation (9), flicker noise, *A* and *K* are proportionally related. In PMOS, *K* value is always 10^{-28} C^2/m^2, and *K* is 50 times smaller than NMOS transistor. Therefore, Flicker noise of PMOS is less than NMOS. For this purpose, we choose PMOS to make Mixer LO signal switch stage and lower down the effect of flicker noises [14].

In addition, when local oscillation signals are input to Mixer, noise impulses will be generated on a switch stage. The flicker noise current is expressed in the following formula:

$$i_{o,n} = \frac{(4I_{sw} \times V_n(f))}{(S_{LO} \times T_{LO})} \propto I_{sw} \quad (10)$$

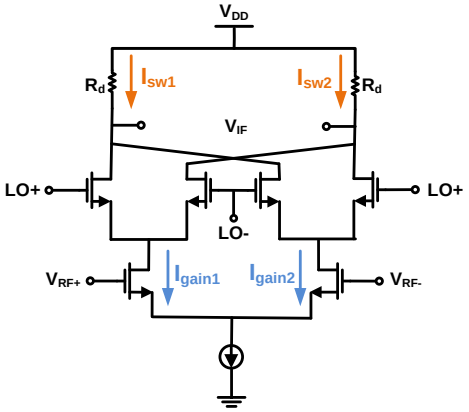
I_{sw}: Mixer switch stage bias voltage current.

V_n: Switch stage Equivalent of flick noise voltage

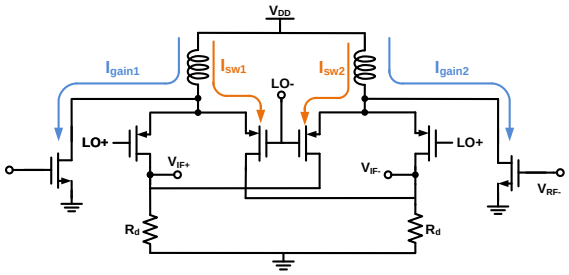
T_{LO}: Cycle Time of Signal LO

S_{LO}: Slope of signal LO

From Equation (10), spectrum of noise current on an input stage is proportional to bias voltage current of a switch stage. Therefore, lowering down I_{sw} is decreasing flicker noise affection. Fig. 6(a) shows traditional double-balance Mixer. Because of switch stage directly cascaded on gain stage, in order to get same gain, switch stage must use same bias voltage current with gain stage, which makes flick noise higher. The proposed architecture is why we use a folded-mixer. The purpose of this architecture shown on Fig. 6(b) is to divide operating bias voltage current between gain and switch stage to achieve high gain and low noise. Comparing with big bias voltage current of gain stage, switch stage only needs smaller bias voltage current to control. Power consumption of the whole system is not to increase, and flick noise is very low.



(a) Double-balance mixer circuit



(b) Folded-cascode mixer circuit

Figure 6: Double-balance mixer and Folded-cascode mixer circuit